256MB – 2x16Mx64 DDR SDRAM SO-DIMM, UNBUFFERED

FEATURES

- Unbuffered Double-data-rate architecture
- DDR300 and DDR400
  - JEDEC design specifications
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2.5, 3
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh, (8K/64ms Refresh)
- Serial presence detect with EEPROM
- Dual Rank
- Power Supply: $V_{CC} = V_{CC}$: 2.5V ± 0.2V (DDR300)
  $V_{CC} = V_{CCQ}$: 2.6V ± 0.1V (DDR400)
- JEDEC standard 200 pin SO-DIMM package
  - Package height options:
    D4: 31.75mm (1.25") TYP

NOTE: Consult factory for availability of:
- RoHS compliant products
- Vendor source control options
- Industrial temperature option

DESCRIPTION

The WV3EG6437S is a 2x16Mx64 Double Data Rate SDRAM memory module based on 256Mb DDR SDRAM components. The module consists of eight 16Mx16 DDR SDRAMs in 66 pin TSOP package mounted on a 200 Pin FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change without notice.

OPERATING FREQUENCIES

	DDR400@CL=3	DDR333@CL=2.5
Clock Speed	200MHz	166MHz
CL-t_{RCD}-t_{RP}	3-3-3	2.5-3-3

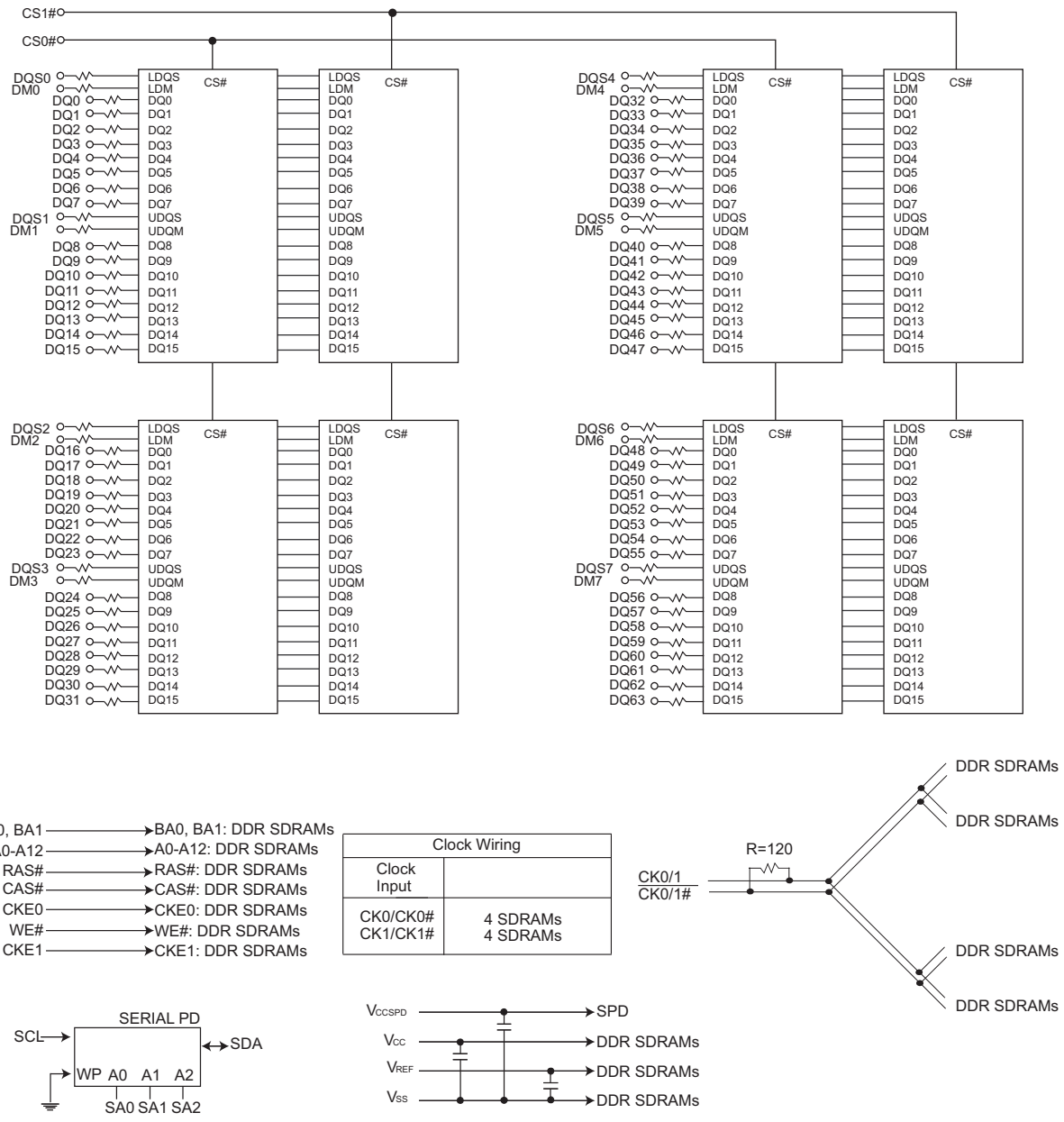
PIN CONFIGURATIONS

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{REF}	51	V_{SS}	101	A9	151	DQ42
2	V_{REF}	52	V_{SS}	102	A8	152	DQ46
3	V_{SS}	53	DQ19	103	V_{SS}	153	DQ43
4	V_{SS}	54	DQ23	104	V_{SS}	154	DQ47
5	DQ0	55	DQ24	105	A7	155	V_{CC}
6	DQ4	56	DQ28	106	A6	156	V_{CC}
7	DQ1	57	V_{CC}	107	A5	157	V_{CC}
8	DQ5	58	V_{CC}	108	A4	158	CK1#
9	V_{CC}	59	DQ25	109	A3	159	V_{SS}
10	V_{CC}	60	DQ29	110	A2	160	CK1
11	DQS0	61	DQS3	111	A1	161	V_{SS}
12	DM0	62	DM3	112	A0	162	V_{SS}
13	DQ2	63	V_{SS}	113	V_{CC}	163	DQ48
14	DQ6	64	V_{SS}	114	V_{CC}	164	DQ52
15	V_{SS}	65	DQ26	115	A10	165	DQ49
16	V_{SS}	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	V_{CC}
18	DQ7	68	DQ31	118	RAS#	168	V_{CC}
19	DQ8	69	V_{CC}	119	WE#	169	DQS6
20	DQ12	70	V_{CC}	120	CAS#	170	DM6
21	V_{CC}	71	NC	121	CS0#	171	DQ50
22	V_{CC}	72	NC	122	CS1#	172	DQ54
23	DQ9	73	NC	123	NC	173	V_{SS}
24	DQ13	74	NC	124	NC	174	V_{SS}
25	DQS1	75	V_{SS}	125	V_{SS}	175	DQ51
26	DM1	76	V_{SS}	126	V_{SS}	176	DQ55
27	V_{SS}	77	NC	127	DQ32	177	DQ56
28	V_{SS}	78	NC	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	V_{CC}
30	DQ14	80	NC	130	DQ37	180	V_{CC}
31	DQ11	81	V_{CC}	131	V_{CC}	181	DQ57
32	DQ15	82	V_{CC}	132	V_{CC}	182	DQ61
33	V_{CC}	83	NC	133	DQS4	183	DQS7
34	V_{CC}	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	V_{SS}
36	V_{CC}	86	NC	136	DQ38	186	V_{SS}
37	CK0#	87	V_{SS}	137	V_{SS}	187	DQ58
38	V_{SS}	88	V_{SS}	138	V_{SS}	188	DQ62
39	V_{SS}	89	NC	139	DQ35	189	DQ59
40	V_{SS}	90	V_{SS}	140	DQ39	190	DQ63
41	DQ16	91	NC	141	DQ40	191	V_{CC}
42	DQ20	92	V_{CC}	142	DQ44	192	V_{CC}
43	DQ17	93	V_{CC}	143	V_{CC}	193	SDA
44	DQ21	94	V_{CC}	144	V_{CC}	194	SA0
45	V_{CC}	95	CKE1	145	DQ41	195	SCL
46	V_{CC}	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	V_{CCSPD}
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	V_{SS}	199	NC
50	DQ22	100	A11	150	V_{SS}	200	NC

PIN NAMES

A0 – A12	Address input
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
DQS0-DQS7	Data Strobe Input/Output
CK0, CK1	Clock Inputs
CK0#, CK1#	
CKE0, CKE1	Clock Enable Inputs
CS0#, CS1#	Chip select Inputs
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DM0-DM7	Data Mask
V_{CC}	Power Supply
V_{SS}	Ground
V_{REF}	Reference Power Supply
V_{CCSPD}	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	SPD clock input
SA0-SA2	SPD address
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



Note: All resistor values are 22 ohms ±5% unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 3.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	-0.5 to 3.6	V
Storage Temperature	T_{STG}	-55 to +150	°C
Operating Temperature	T_A	0 - 70	°C
Power Dissipation	P_D	8	W
Short Circuit Current	I_{OS}	50	mA

Note:

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC CHARACTERISTICS

$0°C \leq T_A \leq 70°C$

Parameter		Symbol	Min	Max	Unit
Supply voltage DDR333		V_{CC}	2.3	2.7	V
I/O Supply voltage DDR333		V_{CCQ}	2.3	2.7	V
Supply Voltage DDR400		V_{CC}	2.5	2.7	V
I/O Supply Voltage DDR400		V_{CCQ}	2.5	2.7	V
I/O Reference voltage		V_{REF}	0.49 + V_{CC}	0.51 + V_{CC}	V
I/O Termination voltage		V_{TT}	V_{REF} - 0.04	V_{REF} + 0.04	V
Input logic high voltage		$V_{IH(DC)}$	V_{REF} + 0.15	V_{CC} + 0.30	V
Input logic low voltage		$V_{IL(DC)}$	-0.3	V_{REF} - 0.15	V
Input voltage level, CK and CK#		$V_{In(DC)}$	-0.3	V_{CC} + 0.30	V
Input differential voltage, CK and CK#		$V_{ID(DC)}$	0.36	V_{CC} + 0.60	V
Input crossing point voltage, CK and CK#		$V_{IX(DC)}$	0.3	V_{CC} + 0.60	V
Input leakage current	Addr, CAS#, RAS#, WE#	I_I	-16	16	µA
	CS#, CKE		-8	8	µA
	CK, CK#		-8	8	µA
	DM		-4	4	µA
Output leackage current	DQ, DQS	I_{OZ}	-10	10	µA
Output high surrent (normal strength) $V_{OUT} = V_{TT} + 0.84V$		I_{OH}	-16.8	-	mA
Output high surrent (normal strength) $V_{OUT} = V_{TT} - 0.84V$		I_{OL}	16.8	-	mA
Output high surrent (half strength) $V_{OUT} = V_{TT} + 0.45V$		I_{OH}	-9	-	mA
Output high surrent (half strength) $V_{OUT} = V_{TT} - 0.45V$		I_{OL}	9	-	mA

Notes:

1. V_{REF} is expected to equal 0.5*V_{CCQ} of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed +/-2 percent of the DC value.
2. V_{TT} in sot applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.
3. V_{ID} is the magnitude of the difference between the input level on CK and the input level of CK#.
4. V_{CCQ} of all IC's are ited to V_{CC}.

AC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min.	Max.	Units	Notes
Input High (Logic1) Voltage	$V_{IH(AC)}$	V_{REF} + 0.31		V	1
Input Low (Logic0) Voltage	$V_{IL(AC)}$		V_{REF} - 0.31	V	1
Input Differential Voltage, CK and CK# input	$V_{ID(AC)}$	0.7	V_{CCQ} + 0.6	V	
Input Crossing Point Voltage, CK and CK# input	$V_{IX(AC)}$	0.5*V_{CC} - 0.2	0.5*V_{CC} + 0.2	V	

Notes:

1. V_{IH} overshoot: V_{IN} = V_{CC} + 1.5V for a pulse width ≤ 3ns and the pulse can not be greater than 1/3 of the cycle rate.
   V_{IL} undershoot: V_{IL} = -1.5V for a pulse width ≤ 3ns and the pulse can not be greater than 1/3 of the cycle rate.

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A12, BA0~BA1, RAS#, CAS#, WE#)	C_{IN1}	20	28	pF
Input Capacitance (CKE0, CKE1)	C_{IN2}	12	16	pF
Input Capacitance (CS0#, CS1#)	C_{IN3}	12	16	pF
Input Capacitance CK, CK0#, CK1, CK1#)	C_{IN4}	12	16	pF
Input Capacitance (DM0 ~ DM7), (DQS0 ~ DQS7)	C_{IN5}	12	14	pF
Input Capacitance (DQ0 ~ DQ63)	C_{OUT1}	12	14	pF

I_{CC} SPECIFICATIONS AND TEST CONDITIONS

Parameter	Symbol	Conditions	DDR403 @CL=3 Max	DDR333 @CL=2.5 Max	Units
Operating Current	I_{CC0}*	One device bank; Active - Precharge; t_{RC}=t_{RC}(MIN); t_{CK}=t_{CK}(MIN); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	456	372	mA
Operating Current	I_{CC1}*	One device bank; Active-Read-Precharge; Burst = 2; t_{RC}=t_{RC}(MIN);t_{CK}=t_{CK}(MIN) ; Iout = 0mA; Address and control inputs changing once per clock cycle.	616	512	mA
Precharge Power-Down Standby Current	I_{CC2P}**	All device banks idle; Power- down mode; t_{CK}=t_{CK}(MIN); CKE=(low)	32	24	mA
Idle Standby Current	I_{CC2F}**	CS# = High; All device banks idle; t_{CK}=t_{CK}(MIN); CKE = high; Address and other control inputs changing once per clock cycle. Vin = Vref for DQ, DQS and DM.	240	240	mA
Active Power-Down Standby Current	I_{CC3P}**	One device bank active; Power-down mode; t_{CK}(MIN); CKE=(low)	400	280	mA
Active Standby Current	I_{CC3N}**	CS# = High; CKE = High; One device bank; Active-Precharge; t_{RC}=t_{RAS}(MAX); t_{CK}=t_{CK}(MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	520	440	mA
Operating Current	I_{CC4R}*	Burst = 2; Reads; Continous burst; One device bank active;Address and control inputs changing once per clock cycle; t_{CK}=t_{CK}(MIN); Iout = 0mA.	736	652	mA
Operating Current	I_{CC4W}**	Burst = 2; Writes; Continous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK}=t_{CK}(MIN); DQ,DM and DQS inputs changing twice per clock cycle.	736	652	mA
Auto Refresh Current	I_{CC5}**	t_{RC}=t_{RC}(MIN)	1,600	1,440	mA
Self Refresh Current	I_{CC6}**	CKE $\leq$ 0.2V	24	24	mA
Operating Current	I_{CC7}*	Four bank interleaving Reads (BL=4) with auto precharge with t_{RC}=t_{RC} (MIN); t_{CK}=t_{CK}(MIN); Address and control inputs change only during Active Read or Write commands.	1,416	1,332	mA

Note: I_{CC} specification is based on SAMSUNG components. Other DRAM Manufacturers specification may be different.

* Value calculated as one module rank in this operation condition, and all other module ranks in I_{CC2P} (CKE LOW) mode.

** Value calculated reflects all module ranks in the operating condition.

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

AC CHARACTERISTICS			403		335		UNITS
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	
Access window of DQs from CK/CK#		t_{AC}	-0.65	+0.65	-0.7	+0.7	ns
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}
Clock cycle time	CL = 3	$t_{CK\ (3)}$	5	10			ns
	CL = 2.5	$t_{CK\ (2.5)}$			6	12	ns
DQ and DM input hold time relative to DQS		t_{DH}	0.40		0.40		ns
DQ and DM input setup time relative to DQS		t_{DS}	0.40		0.40		ns
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75		1.75		ns
Access window of DQS from CK/CK#		t_{DQSCK}	-0.55	+0.65	-0.60	+0.60	ns
DQS input high pulse width		t_{DQSH}	0.35		0.35		t_{CK}
DQS input low pulse width		t_{DQSL}	0.35		0.35		t_{CK}
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}		0.40		0.45	ns
Write command to first DQS latching transition		t_{DQSS}	0.72	1.28	0.75	1.25	t_{CK}
DQS falling edge to CK rising - setup time		t_{DSS}	0.20		0.20		t_{CK}
DQS falling edge from CK rising - hold time		t_{DSH}	0.20		0.20		t_{CK}
Half clock period		t_{HP}	$t_{CH(MIN)}$ or $t_{CL(MIN)}$		$t_{CH(MIN)}$ or $_{(MIN)}$		ns
Data-out high-impedance window from CK/CK#		t_{HZ}		+0.65		+0.70	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.65		-0.70		ns
Address and control input hold time (1 V/ns)		t_{IHF}	0.60		0.75		ns
Address and control input setup time (1 V/ns)		t_{ISF}	0.60		0.75		ns
Address and control input hold time (0.5 V/ns)		t_{IHS}	0.70		0.80		ns
Address and control input setup time (0.5 V/ns)		t_{ISS}	0.70		0.75		ns
Address and Control input pulse width (for each input)		t_{IPW}	2.20		2.20		ns
LOAD MODE REGISTER command cycle time		t_{MRD}	10		10		ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns
Data hold skew factor		t_{QHS}		0.50		0.55	ns
ACTIVE to PRECHARGE command		t_{RAS}	40	70K	42	70K	ns
ACTIVE to READ with Auto precharge command		t_{RAP}	15		18		ns
ACTIVE to ACTIVE/AUTO REFRESH command period		t_{RC}	55		60		ns
AUTO REFRESH command period		t_{RFC}	70		72		ns
ACTIVE to READ or WRITE delay		t_{RCD}	15		18		ns
PRECHARGE command period		t_{RP}	15		18		ns
DQS read preamble		t_{RPRE}	0.90	1.10	0.9	1.10	t_{CK}
DQS read postamble		t_{RPST}	0.40	0.60	0.4	0.60	t_{CK}
ACTIVE bank a to ACTIVE bank b command		t_{RRD}	10		12		ns
DQS write preamble		t_{WPRE}	0.25		0.25		t_{CK}
DQS write preamble setup time		t_{WPRES}	0		0		ns

Note: AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

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DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

AC CHARACTERISTICS		403		355		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS
DQS write postamble	t_{WPST}	0.40	0.60	0.40	0.60	t_{CK}
Write recovery time	t_{WR}	15		15		ns
Internal WRITE to READ command delay	t_{WTR}	2		1		t_{CK}
Average periodic refresh interval	t_{REFI}		7.80		7.80	µs
Exit SELF REFRESH to non-READ command	t_{XSNR}	75		75		ns
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		t_{CK}
Auto precharge write recovery + precharge time	t_{RAL}	t_{WR}/t_{CK} +t_{RP}/t_{CK}		t_{WR}/t_{CK} +t_{RP}/t_{CK}		t_{CK}

Note: AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

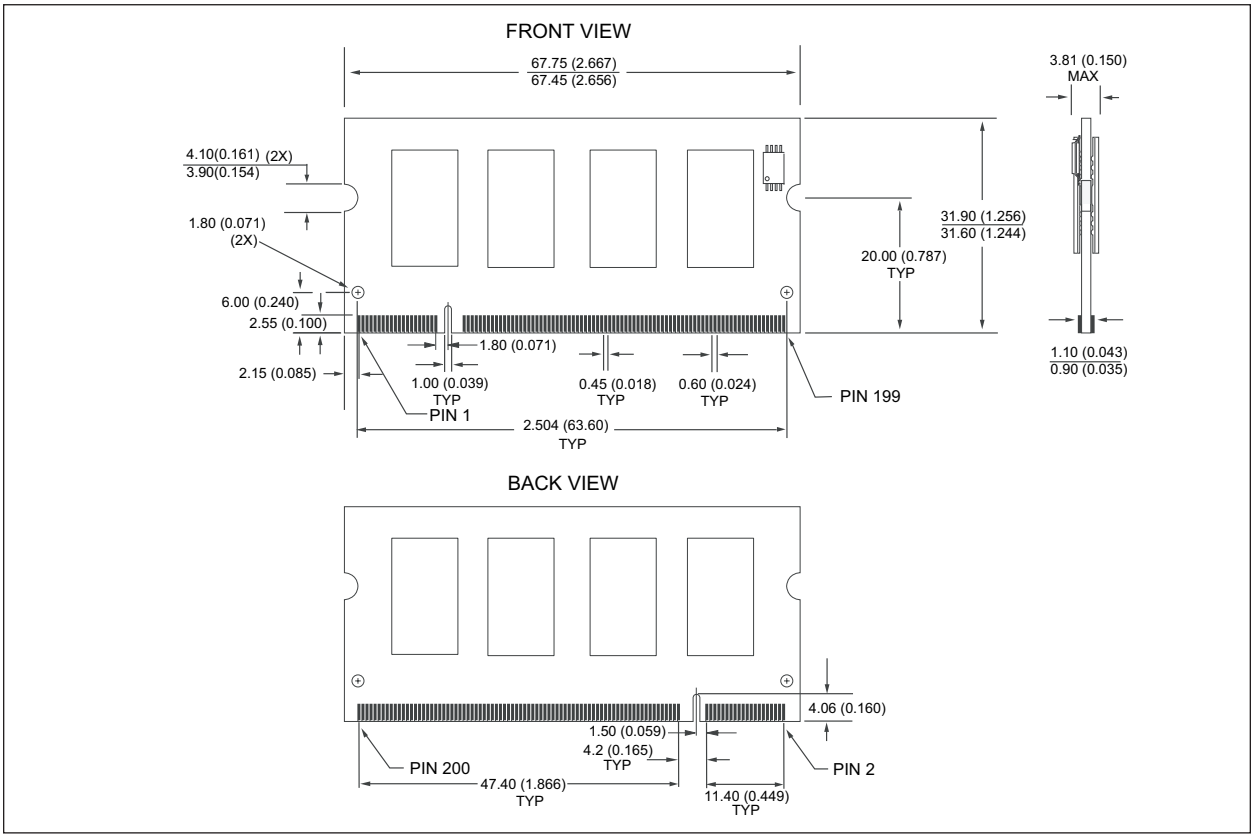
ORDERING INFORMATION FOR D4

Part Number	Speed/Data Rate Frequency	Height*
WV3EG6437S403D4xxG	200MHz/400Mbps, CL=3	31.75 (1.25") TYP
WV3EG6437S335D4xxG	166MHz/333Mbps, CL=2.5	31.75 (1.25") TYP

NOTES:

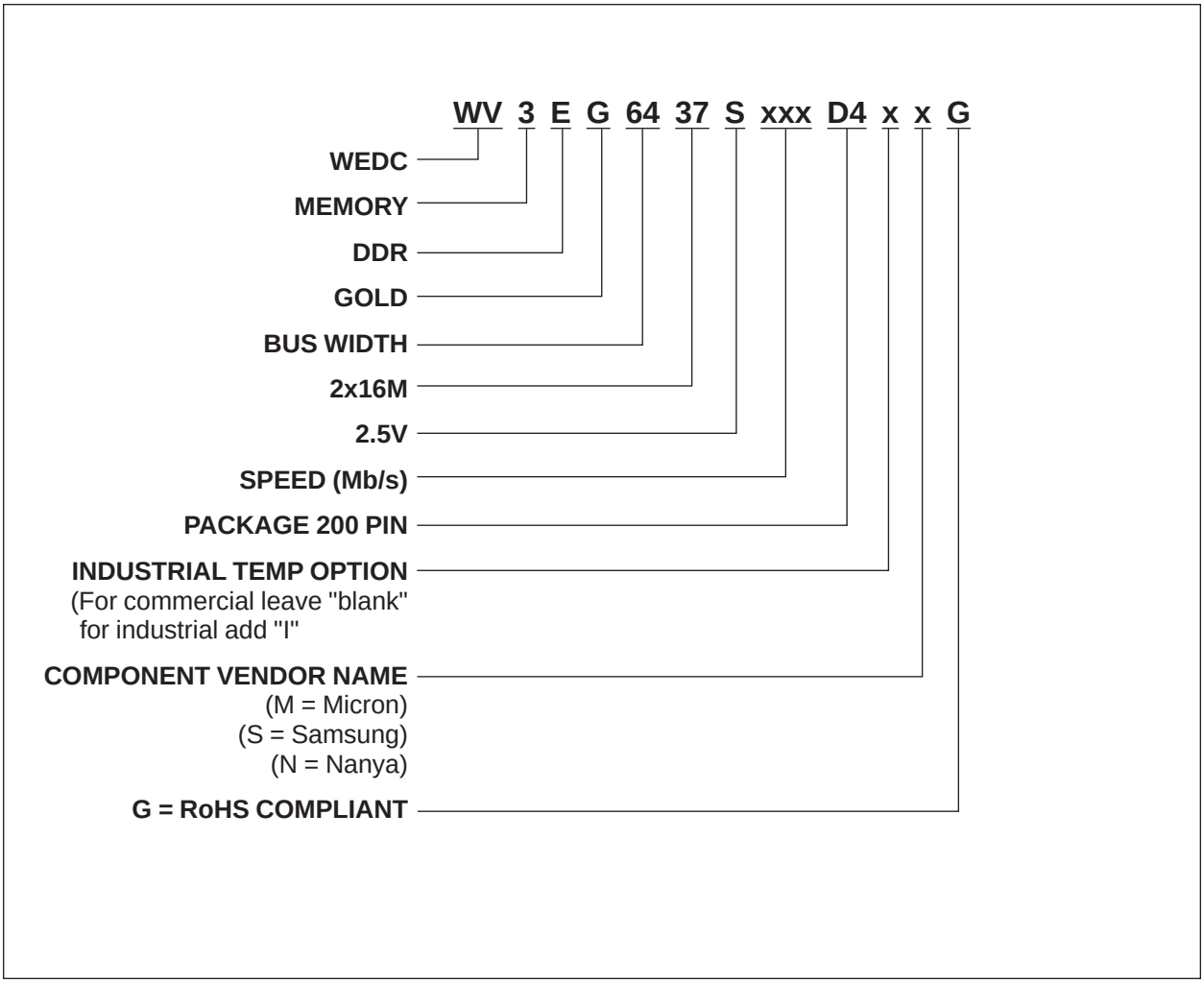
- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D4



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

256MB – 32Mx64, DDR SDRAM UNBUFFERED

DRAM DIE OPTIONS:

- SAMSUNG: H-Die (K4H561638H-UCB3) RoHS
- MICRON: T26A: F-Die

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	June 2006	Advanced